REMARKS

The Official Action dated August 10, 2005 has been received and its contents carefully noted. In view thereof, claims 1-5 have been amended in order to better define that which Applicant regards as the invention. As previously, claims 1-5 are presently pending in the instant application.

With reference now to the Official Action and particularly paragraphs 2 and 4 thereof, claims 1, 3 and 5 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,164,970 issued to Shin et al. while claims 2 and 4 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shin et al. Each of these rejections are respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As can be seen from the foregoing amendments, independent claim 1 has been amended to recite a variable driving circuit comprising a shift register configured by a cascade connection of D-type flip-flops, wherein the D-type flip-flops respectfully generate output signals and a selecting circuit which selects any one of the output signals as an output signal of the variable dividing circuit, wherein the D-type flip-flops are respectively reset by the selected one of the output signals. That is, with the present invention, the D-type flip-flop circuits are reset by the selected one of the output circuits from the D-type flip-flop circuits. To the contrary, Shin et al. teaches that the shift register 5 has a plurality of switches S1, S2 and S3 for selecting one of the Q outputs from the (N-3)-th flip-flop 17, the (N-2)-th flip-flop 18 and the (N-1)-th flip-flop 19. However, Shin et al. is silent with respect to the flip-flop 17-19 being respectively reset by the selected one of the Q outputs. That is, while Shin et al. may disclose that the D-type flip-flops have D(data), S(set), R(reset) and clock input terminals, this reference fails to disclose or remotely suggest that the D-type flip-flops are

respectively reset by the selected one of the output signals as is specifically recited by Applicant's claimed invention. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in independent claim 1 as well as those claims which depend therefrom clearly distinguishes over the teachings of Shin et al. and is in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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